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(73) Proprietor: **RAMTRON INTERNATIONAL CORPORATION**
1850 Ramtron Drive
Colorado Springs, Colorado 80921(US)

(72) Inventor: **Eaton Jr., Sheffield S.**
3361, Spring Ridge Circle
Colorado Springs Colorado 80906(US)
Inventor: **Parris, Michael C.**
3160 Venable Pass Court
Colorado Springs Colorado 80917(US)

(74) Representative: **Driver, Virginia Rozanne et al**
Page White & Farrer
54 Doughty Street
London WC1N 2LS (GB)

Rank Xerox (UK) Business Services
(3. 10/3.6/3.3. 1)

Description

The present invention relates to capacitor circuits and particularly their application to memory circuitry.

The present invention in one of its aspects relates to capacitance circuits and particularly to ferroelectric capacitors. Ferroelectric capacitors and uses thereof in memory circuitry are described in United States Patent No. 4,809,225 in the name of Klaus Dimmler and S. Sheffield Eaton, Jr. (one of the inventors hereof), entitled "Ferroelectric Shadow RAM," filed simultaneously herewith and in several issued U.S. patents such as Rohrer U.S. Patent 3,728,694 for "Thin Film Ferroelectric Device" and Rohrer U.S. Patent 3,939,292 for "Process For Stable Phase III Potassium Nitrate And Articles Prepared Therefrom."

A certain combination of two ferroelectric capacitors having a common node has been referred to as a "transcharger" or a "transpolarizer" in Polar Dielectrics by Burfoot and Taylor, pp. 291-93 (1979). This text indicates such transchargers as having a "blocked" state and an "unblocked" state. No specific mention is made in this reference of using such a configuration as a capacitance divider or of combining it with other circuit elements to form a memory cell, although it is reported that transchargers had been used to form "an associative memory."

By way of example of such a transpolarizer, reference is made to US-A-3508213 which discloses a capacitance divider comprising two series coupled ferroelectric capacitors in which data is stored by polarizing the capacitors. The data state can be sensed by applying a high voltage across the capacitors and detecting whether the resulting current flow is large (unblocked) or small (blocked).

Reference is also made to IBM Technical Disclosure Bulletin, Vol. 24 No. 5, Oct. 1981 which discloses a memory cell having a volatile and a non-volatile portion.

An object of this invention is to employ an arrangement of ferroelectric capacitors as a capacitance divider useful in memory applications and elsewhere.

According to a first aspect of the present invention there is provided a method of reading and writing digital data in a non-volatile memory comprising steps of:

writing the digital data by polarizing a first pair of ferroelectric capacitors coupled in series, said first pair of capacitors having a common node and first and second poles, to polarize ferroelectric material in the capacitors to correspond to the data; and

reading the data by developing a voltage at said common node by applying a voltage transition to only one of said poles; characterised by the step of sensing said voltage at said common node, and in that said step of polarizing includes applying a voltage representing the data to said common node while applying a first voltage corresponding to one data state to said two poles together and then applying a second voltage corresponding to the other data state to said two poles together.

Other aspects of the present invention seek to provide a ferroelectric memory cell wherein decay of the ferroelectric properties is self-compensated; and a "shadow" RAM which is an improvement of the circuit described in the above-referenced Ferroelectric Shadow RAM patent application.

The invention also provides a shadow dynamic RAM cell and an improved dynamic RAM cell capable of use in both volatile and non-volatile modes.

According to a second aspect of the present invention there is provided a semiconductor memory comprising a memory cell and associated control circuitry, the memory cell including a capacitance divider formed by first and second ferroelectric capacitors in series to provide a common node coupled to plates of both of said ferroelectric capacitors and to provide first and second poles coupled to the other two plates of said ferroelectric capacitors, wherein the capacitance divider forms a non-volatile memory cell portion of the memory cell, and wherein said control circuitry provides first and second output signals supplied respectively to the first and second poles of said capacitance divider, the arrangement being such that the remnant polarization of the ferroelectric material in said ferroelectric capacitors represents the non-volatile stored data characterised in that the memory cell further comprises a volatile memory cell portion arranged to store data on an internal node thereof, said common node of said capacitance divider being coupled to said internal node of said volatile portion; and in that said control circuitry is operable to produce said first and second output signals to cause data to be stored in said non-volatile portion by applying a first voltage corresponding to one data state to said first and second poles together while allowing the common node to be connected to said internal node and then applying a second voltage corresponding to the other data state to said first and second poles together.

According to a third aspect of the present invention there is provided a semiconductor memory array comprising a plurality of memory cells and associated control circuitry the memory cells each including a non-volatile memory cell portion including a capacitance divider formed by first and second ferroelectric capacitors in series to provide a common node coupled to plates of both of said ferroelectric capacitors and to provide first and

second poles coupled to the other two plates of said ferroelectric capacitors wherein the memory array comprises:

a plurality of bit lines defining columns;

a plurality of word lines defining rows orthogonal to said bit lines;

said plurality of memory cells being located at crossings of said word lines and said bit lines and each cell characterised by including a volatile memory cell portion coupled to the common node of the non-volatile memory cell portion; and by

said memory array further including a plurality of pairs of conductive common lines, one pair corresponding to one of said word lines, wherein one of said common lines in the pair is coupled to said first poles in said memory cells along the row, and the other of said common lines of the pair being coupled to said second poles in the memory cells along the row, whereby distinct voltages can be applied to said first and second poles separately along a selected row; wherein said associated control circuitry is operable to produce said distinct voltages to cause data to be stored in said non-volatile portion by applying a first voltage corresponding to one data state to said first and second poles together while allowing the common node to be connected to said internal node and then applying a second voltage corresponding to the other data state to said first and second poles together.

Thus, according to a first aspect of the present invention, a circuit element is formed by coupling two ferroelectric capacitors, which preferably but not necessarily are substantially identical in physical construction and size, in series. Three accessible points result: two outside points referred to herein as "poles" and a common node between the capacitors. That is, the common node is electrically coupled to both capacitors, while the poles are coupled to only one capacitor each. This circuit is referred to herein as a programmable capacitance divider. The ferroelectric states of the two capacitors are set so that dipoles therein are oriented essentially uniformly with respect to the common node. Subsequently a voltage pulse is placed along one of the poles while the other pole is fixed at a reference voltage, such as ground, while the common node is permitted to float. A voltage develops at the common node which indicates the prior polarization of the ferroelectric materials in the divider.

According to the second aspect of the present invention, this circuit element is used in an otherwise volatile memory cell to form a non-volatile portion, referred to as a "shadow" portion. In one embodiment, a static RAM cell formed by a CMOS flip-flop has two nodes. Each node is coupled to a respective common node of a series arrangement of ferroelectric capacitors as described supra. Preferably, the volatile static RAM cell internal nodes are coupled by the source-drain paths of corresponding access transistors to such common nodes. To store information from the volatile cell into the ferroelectric circuits, the access transistors are turned on and the ferroelectric capacitors are all written into stable polarization states determined by the data content in the volatile cell. Power may then be removed from the circuit, but the ferroelectric states will remain in accordance with the hysteresis property of ferroelectric materials. Thereafter, the capacitor dividers can be pulsed at similar poles. As described above, this causes voltages to be developed at each common node. Because the two voltage dividers will have been previously programmed in complementary states, when voltage pulses are applied to similar poles, there will be a difference between the resulting common node voltages. This difference will be sensed by the flip-flop portion of the volatile cell and restore the data thereto.

Another aspect of the present invention relates to the combining of the invented programmable capacitance divider with an otherwise volatile dynamic RAM cell, thereby forming a nonvolatile portion. The dynamic RAM cell may comprise a single transistor, single capacitor cell, or any other dynamic RAM cell. The nonvolatile portion combines a programmable capacitance divider as described above via a coupling transistor, the source-drain path of which couples the plate of the dynamic RAM capacitor to the common node of the programmable capacitance divider. The DRAM cell is read so that the voltage impressed on the bit line from reading the cell becomes available to program the divider. While the dynamic RAM cell is being read, the coupling transistor to the ferroelectric circuit is turned on. Its two poles are coupled to receive a voltage pulse starting at zero volts which rises thereafter to five volts. If the data in the DRAM cell corresponded to a high voltage stored on the memory cell capacitor, then when the coupling transistor is turned on, the high voltage from the volatile portion of the DRAM cell is applied to the common node of the capacitance divider. When the other two poles of the divider are at zero volts, both ferroelectric capacitors will be written into a polarization state determined by that set of conditions. When the voltage rises, to five volts, for example, on the other poles of the divider, no polarization change occurs because equal voltages are applied across the ferroelectric capacitors. If, on the other hand, the voltage in the dynamic RAM cell was low, such as zero volts, then zero volts will be applied from the volatile part of the DRAM cell to the common node of the divider. When the zero volts signal is applied to the two poles of the

divider, no polarization occurs because zero volts is across each of the two ferroelectric capacitors. However, when the voltage pulse on the other two poles rises to five volts, both ferroelectric capacitors are written into a state corresponding thereto. At this point the data is stored in the nonvolatile ferroelectric capacitor circuit, and power can be removed from the DRAM cell without losing data. To restore the data to the DRAM cell from the divider portion, with the coupling transistor to the ferroelectric capacitors turned off, one of the poles is grounded and the other one is pulsed from zero volts to a high voltage such as +5 volts. As described above, the voltage at the common node will be lower than the midpoint voltage if one logic state was programmed previously, but higher than the midpoint voltage for the other state. At this time, the coupling transistor is turned on so that this voltage at the common node is transferred to the DRAM cell. Then the coupling transistor preferably is turned off and the DRAM cell is read in the customary fashion.

According to another aspect of this invention, the programmable capacitance divider is employed as the memory element of a memory cell. That is, it is not a "shadow" portion but instead is the primary memory apparatus. Such structure operates, at separate times, in the volatile and nonvolatile modes.

A preferred embodiment of the present invention provides a small area, high capacity memory cell by using PZT as a dielectric material.

A further appreciation of the several aspects of the present invention will be gained by considering the following detailed description of preferred embodiments in conjunction with accompanying drawings wherein:

Figure 1 is a sketch representative of a hysteresis loop exhibited by ferroelectric materials;

Figure 2A represents schematically a pair of capacitors in series;

Figure 2B illustrates the same circuit arrangement of Figure 2A, but is redrawn to show the three connection points more clearly;

Figure 2C illustrates the polarization in one logic state

Figures 3A and 3B show how the programmable capacitance divider of the present invention is applied to form a "shadow" static RAM cell;

Figures 4A and 4B are schematic diagrams illustrating how a programmable capacitance divider of the present invention is applied to form a "shadow" dynamic RAM cell;

Figure 5 shows another embodiment of the present invention using the programmable capacitance divider in a memory cell, but not as a "shadow" portion.

Figure 6 shows a small array of memory cells using programmable capacitance dividers in accordance with the present invention;

Figures 7 and 8 show timing diagrams for the circuit of Fig. 6; and

Figure 9 illustrates a simple one-transistor memory cell for a DRAM in which PZT can be used as a dielectric to develop a dramatic improvement over current high-performance DRAM cells.

Figure 1 illustrates a hysteresis curve of the type commonly associated with ferroelectric materials. The X axis, or abscissa, may represent voltage applied across the ferroelectric material, and the Y axis, or ordinate, may represent the resulting polarization. It will be seen that two stable states, A and B, exist even when no voltage is applied across the ferroelectric material. This is because the prior history of the voltage applied across the ferroelectric material determines the stable state A or B which results when voltage is removed. For example, if a material begins at state A and a positive voltage is applied across it, the polarization will increase up to a position not appreciably higher than the Y component of point B. If the voltage is then removed, the polarization remains at point B. A ferroelectric capacitor uses a ferroelectric material as the dielectric between the capacitor plates. U.S. Patent 3,728,694 illustrates the use of ferroelectric materials in devices such as capacitors. United States Serial No. 069,390, "Ferroelectric Shadow RAM," referenced more fully above, shows the use of ferroelectric capacitors to a volatile static RAM cell. The ferroelectric material may comprise lead zirconate titanate or other compounds or mixtures or the like which exhibit ferroelectric properties.

Figure 2A schematically illustrates a divider 10 formed by two capacitors 12, 14 connected in series. This arrangement has a common node 16 between capacitors 12, 14, and poles 18, 20 each corresponding uniquely to only one respective capacitor. Figure 2B illustrates the same arrangement, but is redrawn in slightly different schematic form to have three leads for the three access points of the divider. It is helpful to refer to the divider in the schematic form shown in Figure 2B.

If capacitors 12, 14 are normal, nonferroelectric capacitors, and a voltage Vx is impressed between terminals 18, 20, then the capacitors operate as a voltage divider so that if the capacitors have equal capacity, the voltage at node 16 will have the value of 0.5 Vx. If the capacitances 12, 14 are unequal, then the voltage V16 at 16 is defined by the following equation:

$$V16 = Vx\,[C12/(C12 + C14)]$$

where C12 represents the capacitance of capacitor 12, and C14 represents the capacitance of capacitor 14.

According to the preferred embodiment of this invention, capacitors 12 and 14 are both ferroelectric capacitors. The polarization of this arrangement will now be considered, referring more particularly to Figure 2C. If poles 18 and 20 are both tied to zero volts and +5 volts is applied to common node 16, then the ferroelectric material in capacitors 12, 14 will become polarized in the same direction relative to node 16. In Figure 2C, arrows 22 indicate the polarization in a "down" direction with respect to node 16, and this direction will represent one logic state. Clearly, another logic state can be obtained by changing the voltages so that common node 16 is at zero volts and poles 18, 20 are plus five volts; under such conditions the polarization will be such that arrows 22 will point toward node 16, i.e., they will be "up" and represent the other logic state.

Assume that the polarization has been arranged to be down as depicted in Figure 2C. If pole 18 is now held at ground, common node 16 permitted to float, and a voltage transition from ground to plus five volts applied to pole 20, then a voltage will be developed at node 16. However, this voltage will not be 2.5 volts, but will depend on the effective capacitance of capacitors 12, 14, which, as mentioned, are physically identical but are ferroelectric in nature. When the plus five volts is applied, the voltage at node 16 tends to rise, and the dipoles in the ferroelectric material in capacitor 14 want to change their polarization state. As the voltage at node 16 rises, dipoles in capacitor 12 experience no tendency to change polarization direction because pole 18 is at ground and node 16 is positive. Capacitor 14 therefore exhibits high capacitance because the dipoles want to change polarization, whereas capacitor 12 exhibits low capacitance because its dipoles tend not to change polarization as the result of the applied voltage pulse. Consulting the aforementioned equation it can be seen that the voltage developed at the common node 16 will be higher than 2.5 volts in the condition where the capacitors 12, 14 were both polarized "up". It will similarly be understood that if the capacitors 12, 14 are both polarized "down," then when a voltage pulse from zero to plus five volts is applied to pole 20 while pole 18 is grounded and node 16 floats, a voltage will develop at node 16 which is below 2.5 volts.

It will therefore be appreciated that the process of setting the polarization of capacitors 12 and 14 both in an "up" direction or a "down" direction effectively programs the capacitance divider 10. That is, upon subsequent application of a pulse, a voltage will be developed at the common node 16 which will be dependent on the direction of polarization of the ferroelectric materials. The common node voltage will be either greater than or less than one-half of the voltage transition in the applied pulse.

This programmable capacitance divider can be applied in memory circuits. Figure 3A illustrates a static RAM cell having volatile and nonvolatile portions, the nonvolatile portion including a programmable capacitance divider as shown in Figure 2B. Figure 3A illustrates a full CMOS static RAM cell of the sort using cross-coupled transistors symbolized by circuits 30 which are located between or define two internal nodes 32, 34. Nodes 32, 34 are conventionally coupled via the source-drain paths of access transistors 34, 36 to a complementary pair of bit lines 38, 40. The gate electrodes of access transistors 34, 36 are both coupled to a word line 42 which is also coupled to adjacent memory cells in the same fashion. The portion of the memory cell of Figure 3 as described so far is identical to the memory cell described and illustrated in co-pending United States Serial No. 069,390. This portion of the static RAM cell is volatile in that if power is removed from circuits 30, the data will be lost. In co-pending Serial No. 069,390, transistors such as coupling transistors 44, 46 couple each internal node, such as 32, 34, to a respective single ferroelectric capacitor. The memory cell of Figure 3A, however, couples internal nodes 32, 34 to respective programmable capacitance dividers 48, 50. Divider 48 includes a common node 52 and poles 54, 56. Divider 50 includes a common node 58 together with poles 60, 62.

A detailed discussion of the manner of storing information in a "shadow" portion of a static RAM cell using a ferroelectric capacitor as the "shadow" cell portion is shown in US Patent No. 4,809,225. Briefly, however, the volatile static RAM cell portion creates voltages at nodes 32, 34. Illustratively, the voltages at the internal nodes 32, 34 of the static RAM will be zero volts (VSS) and +5 volts (VCC). Coupling transistors 44, 46 are selectively activated whenever the information from the volatile part of the cell is to be written or restored into the nonvolatile portion of the cell. This polarizes the ferroelectric capacitors.

In the operation of the Figure 3A circuit, when coupling transitors 44, 46 turn on, poles 54, 56, 60, and 62 are grounded so that whichever node 32 or 34 has the high voltage level will polarize the ferroelectric material in its corresponding divider 48 or 50 in the direction shown in Figure 2C (because there will be a voltage across both capacitors of the divider). The internal node 32, or 34 which has zero volts will not result in polarization of its corresponding divider 48 or 50 at this time (because all plates of the divider have zero volts on them). However,

after poles 54, 56, 60, and 62 are coupled to a zero voltage level and one divider becomes polarized, a full VCC level is applied to all poles. The result is that whichever divider 48 or 50 has already been programmed in the "down" direction will not change polarization (because it will have +5 volts at all three of its terminals). However, the other divider will now become polarized in the "up" direction because the internal node from the volatile portion of the cell will couple zero volts to the common node, and the poles of the divider will have the full VCC level impressed thereon. This causes polarization in the "up" direction. At this time, dividers 48 and 50 are programmed in accordance with the data stored in the volatile portion of the SRAM memory cell, and power may be removed from the memory cell safely. Although the voltages will disappear from dividers 48 and 50, the polarizations will remain intact notwithstanding the loss of power.

To restore data from the non-volatile portion to the volatile portion, the following steps occur. Poles 54 and 60 are grounded, and poles 56 and 62 each are brought high (i.e., to VCC). As explained with reference to Figure 2B, each capacitance divider 48, 50 will develop a respective voltage at its common node 52, 58 in accordance with the polarization of the ferroelectric materials between the plates of the capacitors. Because the polarizations of the two dividers 48, 50 will be in opposing directions in accordance with the complementary data at internal nodes 32, 34 of the flip-flop, one of the capacitance dividers will develop a voltage greater than 2.5 volts and the other will develop a voltage below 2.5 volts, assuming that a VCC pulse of 5 volts is applied at poles 56 and 62. Coupling transistors 44, 46 can be turned on at that time, and the volatile portion of the memory cell can then be latched to sense the difference in voltage on common nodes 52, 58, driving one of the internal nodes 32, 34 to ground and the other one to VCC.

The ordinarily skilled artisan will have no difficulty in providing a signal generator to provide the appropriate clock signals for poles 54, 56, 60, and 62, and a signal generator 64 is shown in Figure 3B providing clock signals CLK 1 and CLK 2. As shown in Figure 3A, poles 54 and 60 each are coupled to signal CLK 1, whereas poles 56 and 62 are coupled to clock signal CLK 2. In the transfer from the volatile portion into the ferroelectric non-volatile portion, signals CLK 1 and CLK 2 have the same voltage levels at the same times and experience a transition from VSS to VCC, thereby permitting dividers 48, 50 to be polarized in complementary senses. In the operation of transferring data from the ferroelectric nonvolatile portion into the volatile portion, CLK 1 and CLK 2 are independent of each other, with CLK 1 grounded and CLK 2 initially grounded but then raised to VCC.

Whereas the embodiment of Figure 3A represents an improvement over commonly-assigned, co-pending Serial No. 069,390, Figure 4A represents a basic non-volatile shadow dynamic RAM cell 70. A traditional DRAM memory cell 72 is included as a portion of cell 70. Portion 72 comprises a storage capacitor 74, one plate of which is usually in the substrate and is grounded. The other plate is coupled through the source-drain path of an access transistor 76 to a bit line 78. The gate electrode of transistor 76 is coupled to and controlled by a word line 79. This specific example of cell portion 72 is merely illustrative: Cell portion 72 may have any construction consistent with operation as a DRAM cell.

However, in cell 70 a programmable capacitance divider 80 is coupled via the source-drain path of a coupling transistor 82 to an internal node 84 within cell portion 72. Transistor 82 includes a gate electrode coupled to and controlled by the signal on a control line 86, which may be regarded as a second word line. Divider 80 is configured and operates in accordance with divider 10 illustrated in Figure 2B and includes a common node 88 with two poles 90, 92. Pole 90 is coupled to a logic signal CLK 3, and pole 92 is coupled to a logic signal CLK 4, both provided by a signal generator 94.

During normal operations of the volatile DRAM portion 72, transistor 82 is turned off. In the example given where transistor 82 is an N-channel device, line 86 (which is coupled to generator 94) is grounded to keep transistor 82 off. To store data in the non-volatile ferroelectric portion of circuit 70, transistor 82 is turned on by raising the voltage on line 86. This couples the common node 88 to internal node 84 of volatile cell portion 72. Because the capacitance of capacitor 74 is small, it cannot be relied upon ordinarily to transfer sufficient charge to common node 88 to achieve polarization. Accordingly, in the store to non-volatile cycle, the DRAM cell 72 is read, preferably prior to turning on transistor 82. As the result, the voltage on bit line 78 becomes available through the source-drain path of transistor 76 and is coupled to common node 88.

Clock signals CLK 3 and CLK 4 during this time have the same value. While cell portion 72 is being read and when transistor 82 is initially turned on, both CLK 3 and CLK 4 are at a ground level (VSS). The data in cell 72 to be stored in divider 80 will require the voltage at internal node 84 to be either high or low, e.g. at VSS or VCC. If internal node 84 has a voltage at VSS level (zero volts), then zero volts is applied across the plates of the two capacitors in divider 80, and no polarization occurs. However, CLK 3 and CLK 4 thereafter are

brought to VCC, and a polarization in the "up" direction (illustratively) thereupon occurs because zero volts is applied to common node 88 whereas both poles 90 and 92 have positive voltages. If, on the other hand, the voltage at internal node 84 is high, such as at VCC, then when that voltage is coupled to common node 88 by transistor 82, the two capacitors in divider 80 will be polarized in a down direction when the voltages at poles 90, 92 are low, at VSS. When CLK 3 and CLK 4 rise to VCC, the polarization will not change because substantially the same voltage will be applied to all access points 88, 90, 92. Consequently, after this voltage transition of CLK 3 and CLK 4, the divider is "programmed" by having a polarization in either the "up" or the "down" direction in accordance with the data from the volatile memory cell portion 72. Power can then be removed, and although voltages will all drop to zero throughout the memory cell, the polarization will remain due to the ferroelectric material in divider 80.

To recall or restore the data from divider 80 to volatile cell portion 72, transistor 82 is kept off and the voltage at pole 90 is kept at ground. That is, CLK 3 is at VSS. CLK 4 applied to pole 92 initially is at VSS but is brought to a full VCC level (illustratively +5 volts). As discussed with reference to Figure 2B, a voltage develops at common node 88 depending upon the polarization state of the ferroelectric material in divider 80. The voltage will be greater than 2.5 volts for one state and lower than 2.5 volts for the other polarization state (where the applied pulse is +5 volts). At this time, transistor 82 may be turned on by bringing up the voltage on line 86. This applies the common node voltage to node 84 within cell portion 72 which is caused to execute a read cycle after transistor 82 is turned off, thereby restoring a full "1" or "0" level to node 84.

Another embodiment of this invention is shown in Fig. 5, which shows a memory cell 100 coupled via a transistor 102 to a bit line BL. Transistor 102 is gated by a word line WL. A common node 104 of a capacitance divider 106 as described supra also is coupled to transistor 102. Poles 108, 110 of divider 106 are shown and are coupled to receive clock signals from a signal generator, such as generator 94. The word line and bit line are as commonly used in a DRAM. The bit line must be precharged, however, to VCC/2 prior to a read operation.

To read cell 100, pole 108 is grounded, and pole 110 is brought illustratively to +5v. As described supra, node 104 will be either greater than +2.5v or less than +2.5v depending on the data content of the cell, assuming the capacitance values of the two ferroelectric capacitors to be equal. The word line WL is then brought high, and the voltage on bit line BL will then be slightly greater or less than +2.5v. This voltage can be compared at a sense amplifier 112 to the voltage on the opposite bit line BL' (which is on the other side of sense amplifier 112) whose voltage will have remained at 2.5v, since no cell will have been connected to it. A normal DRAM read operation then occurs to sense the data.

To write data into cell 100, the operation is the same as that of the shadow DRAM cell of Fig. 4A herein. However, no second transistor is needed. The common node 104 becomes coupled to bit line BL via the source-drain path of transistor 102, and poles 108, 110 are held (by clock signals for example) to ground level, VSS. Then poles 108, 110 are brought to VCC. As described supra, the data to be stored will determine the voltage on bit line BL and therefore will determine the polarization of divider 106, i.e. "up" or "down." This programs the divider.

Figure 6 illustrates a simplified version of an array using the programmable capacitance divider arrangement illustrated in Figure 5. As shown in Figure 6, four such cells 120, 122, 124, and 126 are shown. Each cell includes a programmable capacitance divider and corresponding connections. In the array of Figure 6, a first word line 130 is coupled to the gate electrodes of the transistors in cells 120, 122. A second word line 132 is coupled to the gate electrodes of cells 124, 126. A first bit line 134 and a second bit line 136 also are illustrated as orthogonal to word lines 130, 132. With respect to memory cells 120 and 122, a first pair of common lines 138, 140 is coupled to corresponding poles of the programmable capacitance divider in cells 120 and 122. A second pair of common lines 142, 144 is coupled to the poles of the programmable capacitance dividers of the lower portion of the array, that is memory cells 124, 126. Illustratively, the common lines are parallel to the word lines.

Figures 7 and 8 are timing diagrams to illustrate the use of this array. Referring to Figure 7, memory cells 120, 122 will be considered. A waveform is shown therein for word line 130, as well as a waveform for either of the bit lines 134, 136. The signals on lines 138 and 140 are also shown. At a time T0, each bit line is precharged to 2.5 volts. At a time T1, line 138 is pulsed to 5 volts for the purpose of developing a signal at the common node of the chosen memory cell (120 or 122). In response, the common node voltage begins to develop, and short time thereafter at time T2, word line 130 is pulsed to +5 volts thereby coupling the common node of each programmable capacitance divider in cells 120, 122 via the source-drain paths of the corresponding transistors to bit lines 134, 136.

A short time thereafter, at time T3, the voltages on bit lines 134, 136 change from 2.5 volts, rising or falling in accordance with the data which was used to program the cells 120, 122. Thereafter, at a time T4, sense amplifiers 146, 148, coupled to bit lines 134, 136 and operating in a differential mode, using either a folded bit line structure or an open bit line structure as is well known in the memory art, latches the signals developed on each of lines 134, 136 to either VCC or VSS, illustrated in Figure 7 as +5 volts or 0 volts respectively.

Thereafter, word line 130 is pulsed even higher to a +7 volt level for the purpose of restoring a full VCC level into the ferroelectric programmable capacitance dividers. Basically, the word line voltage is elevated more than a threshold voltage over VCC so that the full VCC level latched by the sense amp can be communicated via the source-drain path without a voltage drop to the common node of the corresponding programmable capacitance divider. Hence, at this time, the data has been latched into the sense amplifier and the restoring operation may commence. During this entire time, line 140 has been grounded.

Accordingly, it is shown in Figure 7 that at time T5 the voltage on line 138 is dropped to ground, like line 140. Hence, all poles of the programmable capacitance dividers in cells 120, 122 are at the same voltage level. At a subsequent time T6, all pole voltages are elevated by impressing a +5 volt signal on each of lines 138, 140 until a time T7. This restores the proper state to the ferroelectric materials in the cells. At a time T8, precharging begins by dropping the word line voltage to ground, and it can be seen that at time T9 the bit line voltages are equilibriated and precharged to +2.5 volts.

Figure 8 illustrates the voltage levels for writing into the cells. This process is virtually identical to the restore operation described supra with the sole exception being that the bit line voltage, initially at 2.5 volts, is driven by appropriate circuitry such as a "Data In" buffer and related amplifiers to either a VCC or VSS voltage illustrated in Figure 8 as +5 volts or 0 volts, typically by-passing the sense amplifiers 146, 148. These bit line voltages endure over times T_A and T_B during which the voltage levels on lines 138, 140 are initially both at 0 volts and then subsequently both elevated to +5 volts, for reasons described above and extensively in the prior portions of this specification.

It was mentioned supra that one of the materials having ferroelectric properties is PZT. It is another aspect of the present invention to use the normal dielectric constant of this ferroelectric material in a DRAM capacitor application, without necessarily using the Ferroelectric nature for non-volatile storage. Consequently, Figure 9 illustrates in schematic diagram form a standard configuration of a dynamic RAM memory cell of the one capacitor, one transistor type. Any other type can be used. This memory cell 160 includes a transistor 162 and a capacitor 164 which preferably uses, however, a ferroelectric material which is preferably PZT. Standard DRAM cells normally do not use ferroelectric materials. The advantage of using PZT in this application resides in the fact that its dielectric constant is on the order of 1,000 whereas the dielectric constant of silicon dioxide is approximately 4. The result of this is extremely beneficial, namely, the capacitance of device 164 increases by a factor of approximately 250 simply by substituting PZT as the dielectric. The advantage of providing such a configuration is that the objective of achieving high capacitance with a small area of silicon is achieved, and one need not resort to alternate techniques such as trench capacitors currently being developed. For example, the area of capacitor 164 of customary shape to achieve a capacitance of approximately .05 picofarads can be on the order of one square micron or less. As shown in Figure 9, the lower plate of capacitor 164 is grounded. An initialization routine is employed for this embodiment wherein the ferroelectric is programmed to the portion of the hysteresis curve connected to point B of Figure 1. Thereafter, no ferroelectric reversals of polarization occur to bring the polarization down to point A of Figure 1.

The preferred material, as mentioned, is PZT which is an ionic compound formed by lead, zirconium, titanium and oxygen. Its formula is $Pb(ZrTi)O_3$. Preferably there is some variation so that some of the molecules have zirconium and no titanium, whereas others do not have zirconium but instead have titanium. Consequently, some of the molecules have the formula $PbZrO_3$ whereas others of the molecules are $PbTiO_3$. Preferably, the mole relationship between the zirconium and the titanium is in the ratio of 54 to 46, although other ratios may be useful to provide both high capacitance as well as high resistance across the capacitor plates and to minimize its piezoelectric effect. Impurities such as niobium or lanthanum can be added, but those dopants need not be included in this application.

As a further aspect of this invention, the memory cell and circuit diagram of Figure 5 can be employed using PZT as the ferroelectric material in a standard, volatile DRAM operation, but also provides the added benefit that after normal DRAM operations are concluded (or at any other convenient time), the information can be stored in a non-volatile manner by pulsing either line 108 or 110. During normal operations, both 108 and 110 are held to ground, and the device functions exactly as described with respect to Figure 9. Thereafter, when it is desired to store the data in a non-volatile

manner, precisely the same structure can be employed with the write timing of Figure 8. Thereafter, the programmable capacitance divider can be read using the timing of Figure 7 to obtain the data, in cooperation with the sense amplifier 112.

In describing the various aspects of the present invention, it has been indicated that during the operation of storing data in the programmable capacitance divider, the voltages applied to the poles, such as poles 18, 20 in Figure 2B, are tied together. In a modification of the process described herein, the two poles can operate independently.

It will be appreciated that either N-channel or P-channel transistors can be used, and either enhancement-type or depletion-type channels can be used in practicing the present invention. Indeed, any switching device can be used for selectively coupling the programmable capacitance divider to any other circuit. Consequently, switching devices which can be used are not limited to field effect transistors, and may include other types of transistors or other devices.

It has been mentioned also that in the preferred embodiment, the two capacitors placed in series have the same physical size and capacitance. Various arrangements may be made departing from this preferred sizing, although it will be understood that the resulting voltages at the common node may vary as a result of an imbalance in the capacitor sizes. However, it may prove advantageous to use unequal capacitance values in the divider for specific applications in order to control the range of voltages obtained at the common node during a recall operation.

An advantage of incorporating a programmable capacitance divider as a "shadow" portion to a memory cell is its self-tracking nature. That is to say, if there is a variation in the dielectric constant, or a degradation over time of the ferroelectric nature of the dielectric material used in the capacitance divider, the change or variation will uniformly affect both capacitors of the divider. Its operation will continue properly because the two capacitors are balanced against each other.

One advantage to the "shadow" approach is that ferroelectric materials which fatigue after a number of read/write cycles can still be used since they are written into or read typically on power-up or power-down. The volatile portion of the cell is used more frequently in such a combination. On the other hand, a ferroelectric material which fatigues after only a large number of cycles permits direct use of the "shadow" portion as shown in Fig. 5. Such ferroelectric materials may be PZT or lead zirconate titanate.

Claims

1. A method of reading and writing digital data in a non-volatile memory comprising steps of:

   writing the digital data by polarizing a first pair of ferroelectric capacitors (12,14) coupled in series, said first pair of capacitors having a common node (16,52,58,88,104) and first and second poles (18,20,54,56,60,62,90,92,108,110), to polarize ferroelectric material in the capacitors to correspond to the data; and

   reading the data by developing a voltage at said common node (16,52,58,88,104) by applying a voltage transition to only one (20,56,62,92,110) of said poles; characterised by the step of sensing said voltage at said common node (16,52,58,88,104), and in that said step of polarizing includes applying a voltage representing the data to said common node (16,52,58,88,104) while applying a first voltage corresponding to one data state to said two poles (18,20,54,56,60,62,90,92,108,110) together and then applying a second voltage corresponding to the other data state to said two poles (18,20,54,56,60,62,90,92,108,110) together.

2. A method according to claim 1 wherein said step of reading the data includes maintaining said first pole (18,54,60,90,108) at said first voltage while applying a voltage transition to said second pole (20,56,62,92,110), said developed voltage being indicative of said digital data.

3. A method according to claim 1 or 2 wherein said voltage applied to said common node (16,52,58,88,104) during said polarizing step is either at ground or an operating level, and wherein said first and second voltages comprise ground and an operating voltage.

4. A method according to any preceding claim, wherein said applying step comprises coupling an internal node (32,84) of a volatile memory cell (72) to said common node (52,88).

5. A method according to any of claims 1 to 3 wherein said sensing step comprises coupling said common node (88) to an internal node (84) of a dynamic RAM memory cell (72) and reading said dynamic RAM cell.

6. A method according to any preceding claim, wherein said step of applying a voltage transition to said second pole (20,56,62,92,110) comprises controlling the voltage on said sec-

ond pole (20,56,62,92,110) so that it initially is at said first voltage and thereafter changes to another level.

7. A method according to claim 1 wherein said step of developing a voltage at said common node (16,52,58,88,104) comprises changing the polarization of only one of said ferroelectric capacitors.

8. A method according to claim 7, wherein said step of changing the polarization comprises controlling the voltage on one (18,54,60,90,108) of said poles to be constant while providing said voltage transition on the other (20,56,62,92,110) of said poles.

9. A method according to claim 6, wherein said step of applying a voltage transition comprises maintaining said first and second poles (18,20,54,56,60,62,90,92,108,110) at ground and then impressing a different voltage on said second pole (20,56,62,92,110) while said first pole (18,54,60,90,108) is still at ground.

10. A method according to claim 2, wherein said step of applying a voltage comprises applying an operating voltage or ground level voltage to said common node (16,52,58,88,104) of said two capacitors (12,14) and said polarizing step further comprises controlling the voltage at said first and second poles (18,20,54,56,60,62,90,92,108,110) of said capacitors (12,14) to change between ground and operating level while said voltage representing the data is applied to said common node (16,52,58,88,104).

11. A method according to claim 10, wherein the voltages are applied to said poles (18,20,54,56,60,62,90,92,108,110) together during said polarizing step.

12. A method according to claim 1 or 2, wherein the polarizing step further comprises storing complementary data by polarizing a second pair of ferroelectric capacitors (50) coupled in series, said second pair of capacitors having a second common node (58) and two further poles (60,62), said polarizing of said second pair of capacitors being in the opposite direction than the polarizing of said first pair of capacitors, and wherein said step of reading the data comprises generating further voltages at said first and second common nodes (52,58) and wherein said sensing step comprises sensing the difference between the voltages at said two common nodes (52,58).

13. A method according to claim 12, wherein said polarizing step comprises holding each pole (54,56,60,62) of said first and second pairs (48,50) of capacitors at ground and changing the voltage on all of said poles (54,56,60,62) to said second voltage while applying voltages representing complementary data to said first and second common nodes (52,58).

14. A method according to claim 13, wherein said generating step comprises grounding both of said first poles (54,60) and applying a voltage transition to said second poles (56,62) together.

15. A method according to claim 14, including applying the same first signals to said first poles (54,60) together and the same second signals to said second poles (56,62) together.

16. A method according to claim 12, further including coupling said first poles (54,60) together and coupling said second poles (56,62) together, and wherein said polarizing step comprises coupling said first and second poles to ground and then to an operating voltage, and wherein said generating step includes coupling said first poles (54,60) to ground and applying a voltage transition to said second poles (56,62).

17. A semiconductor memory comprising a memory cell (70,100) and associated control circuitry (64,94), the memory cell including a capacitance divider (48,80,106) formed by first and second ferroelectric capacitors in series to provide a common node (52,88,104) coupled to plates of both of said ferroelectric capacitors and to provide first (54,90,108) and second (56,92,110) poles coupled to the other two plates of said ferroelectric capacitors, wherein the capacitance divider (48,80,106) forms a non-volatile memory cell portion of the memory cell, and wherein said control circuitry (64,94) provides first (CLK1,CLK3) and second (CLK2,CLK4) output signals supplied respectively to the first (54,90,108) and second (56,92,110) poles of said capacitance divider, the arrangement being such that the remnant polarization of the ferroelectric material in said ferroelectric capacitors represents the non-volatile stored data characterised in that the memory cell further comprises a volatile memory cell portion (72) arranged to store data on an internal node (32,84) thereof, said common node (52,88,104) of said capacitance divider being coupled to said internal node (32,84) of said volatile portion; and in that said control

circuitry is operable to produce said first and second output signals to cause data to be stored in said non-volatile portion by applying a first voltage corresponding to one data state to said first and second poles together while allowing the common node (52,88,104) to be connected to said internal node (32,84) and then applying a second voltage corresponding to the other data state to said first and second poles together.

18. A semiconductor memory according to claim 17, wherein said volatile memory cell portion (72) is responsively coupled to a word line and coupled to a bit line.

19. A semiconductor memory according to claim 17, wherein the volatile memory cell portion has first (32) and second (34) internal nodes, coupled to respective complementary bit lines and wherein the non-volatile memory cell portion comprises first (48) and second (50) such ferroelectric capacitor dividers, said common nodes (52,58) of said first and second dividers being coupled to said first and second internal nodes respectively, said control circuitry (64) comprising a signal generator being coupled to provide a first variable signal (CLK1) and a second variable signal (CLK2) on first and second outputs, said first variable signal being coupled to one pole (54) of said first capacitance divider and one pole (60) of said second capacitance divider and the second variable signal being coupled to the other poles (56,62) of said first and second capacitance dividers.

20. A semiconductor memory according to claim 19, further including a first coupling transistor (44) having a path of controllable conductivity coupling said common node (52) of said first capacitance divider (48) to one (32) of said internal nodes; and

a second coupling transistor (46) having a path of controllable conductivity, coupling said common node (58) of said second capacitance divider (50) to the other (34) of said internal nodes.

21. A semiconductor memory according to claim 19 or 20, further comprising first (35) and second (36) access transistors, and a word line, one of said bit lines being coupled to a first one (32) of said internal nodes via the souce-drain path of said first access transistor (35), the other of said bit lines being coupled to a second one (34) of said internal nodes, by the source-drain path of said second access transistor (36), said word line being coupled to the gate electrodes of said first and second access transistors, whereby said memory cell is selected when said word line turns on said first and second access transistors thereby to couple the bit lines to said internal nodes.

22. A semiconductor memory according to claim 17, wherein said volatile memory cell portion (72) is coupled to a bit line and a word line and comprises a transistor (76) coupled to a storage capacitor (74), said internal node (84) being connected between said transistor (76) and said storage capacitor (74).

23. A semiconductor memory according to claim 22, which comprises a switching device (82) having a path of controllable conductivity coupled between said common node (88) and said internal node (84) of the volatile memory cell portion.

24. A semiconductor memory according to claim 23, wherein said switching device (82) comprises a field effect transistor having a source, drain, and gate, and wherein said source-drain path is coupled between said common node (88) and said internal node (84) of the volatile memory cell portion (72).

25. A semiconductor memory according to claim 17, wherein said volatile memory cell portion comprises a transistor (102), said transistor coupling said non-volatile portion to a bit line, and said transistor (102) being responsively coupled to a word line.

26. A semiconductor memory according to claim 25, wherein said ferroelectric material comprises PZT.

27. A semiconductor memory array comprising a plurality of memory cells (120,122,124,126) and associated control circuitry the memory cells each including a non-volatile memory cell portion including a capacitance divider (48,80,106) formed by first and second ferroelectric capacitors in series to provide a common node (52,88,104) coupled to plates of both of said ferroelectric capacitors and to provide first (54,90,108) and second (56,92,110) poles coupled to the other two plates of said ferroelectric capacitors wherein the memory array comprises:

a plurality of bit lines (134,136) defining columns;

a plurality of word lines (130,132) defining rows orthogonal to said bit lines;

said plurality of memory cells

(120,122,124,126) being located at crossings of said word lines and said bit lines and each cell characterised by including a volatile memory cell portion coupled to the common node of the non-volatile memory cell portion; and by

said memory array further including a plurality of pairs of conductive common lines (138,140,142,144), one pair (138,140) corresponding to one of said word lines (130), wherein one of said common lines (138) in the pair is coupled to said first poles (54,90,108) in said memory cells along the row, and the other (140) of said common lines of the pair being coupled to said second poles (56,92,110) in the memory cells along the row, whereby distinct voltages can be applied to said first and second poles separately along a selected row; wherein said associated control circuitry is operable to produce said distinct voltages to cause data to be stored in said non-volatile portion by applying a first voltage corresponding to one data state to said first and second poles together while allowing the common node (52,88,104) to be connected to said internal node (32,84) and then applying a second voltage corresponding to the other data state to said first and second poles together.

28. A semiconductor memory array according to claim 27, wherein said volatile memory cell portions each comprise a field effect transistor having a gate electrode coupled to the corresponding word lines (130,132), the source-drain path of said transistor coupling said corresponding bit line (134,136) to the corresponding common node.

29. A semiconductor memory according to claim 27 or claim 28, wherein said associated control circuitry (64,94) comprises a signal generator providing at least one selectively variable signal (CLK1) coupled by one (138) of said pair of conductive common lines to a pole of said capacitance divider.

Patentansprüche

1. Verfahren zum Lesen und Schreiben digitaler Daten in einen Dauerspeicher, mit den Schritten:
Schreiben der digitalen Daten durch Polarisierung eines ersten Paares in Reihe geschalteter ferroelektrischer Kondensatoren (12, 14), wobei das erste Kondensatorenpaar einen gemeinsamen Verzweigungspunkt (16, 52, 58, 88, 104) und einen ersten und einen zweiten Pol (18, 20, 54, 56, 60, 62, 90, 92, 108, 110) aufweist, um ferroelektrisches Material in den Kondensatoren zu polarisieren, so daß es den Daten entspricht; und
Lesen der Daten durch Ausbilden einer Spannung an dem gemeinsamen Verzweigungspunkt (16, 52, 58, 88, 104) durch Aufbringen eines Spannungsübergangs an nur einen der Pole (20, 56, 62, 92, 110), gekennzeichnet durch den Schritt Erfassen der Spannung an dem gemeinsamen Verzweigungspunkt (16, 52, 58, 88, 104) und dadurch, daß der Polarisierungsschritt das Anlegen einer die Daten darstellenden Spannung an den gemeinsamen Verzweigungspunkt (16, 52, 58, 88, 104) enthält, während eine erste Spannung, die einem Datenzustand entspricht, an beide Pole (18, 20, 54, 56, 60, 62, 90, 92, 108, 110) gemeinsam angelegt wird und anschließend eine zweite Spannung, die dem anderen Datenzustand entspricht, an die beiden Pole (18, 20, 54, 56, 60, 62, 90, 92, 108, 110) gemeinsam angelegt wird.

2. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß der Daten-Lese-Schritt das Halten des ersten Pols (18, 54, 60, 90, 108) auf der ersten Spannung umfaßt, während ein Spannungsübergang auf den zweiten Pol (20, 56, 62, 92, 110) aufgebracht wird, wobei die ausgebildete Spannung repräsentativ für die digitalen Daten ist.

3. Verfahren nach den Ansprüchen 1 oder 2, dadurch gekennzeichnet, daß sich die während des Polarisierungsschrittes an den gemeinsamen Verzweigungspunkt (16, 52, 58, 88, 104) angelegte Spannung entweder auf Erd- oder Betriebsniveau befindet und daß die erste und zweite Spannung Erd- und Betriebsspannung aufweisen.

4. Verfahren nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß der Anlegeschritt das Koppeln eines inneren Verzweigungspunktes (32, 84) einer leistungsabhängigen Speicherzelle (72) mit dem gemeinsamen Verzweigungspunkt (52, 88) umfaßt.

5. Verfahren nach einem der Ansprüche 1-3, dadurch gekennzeichnet, daß der Erfassungsschritt das Koppeln des gemeinsamen Verzweigungspunktes (88) mit einem inneren Verzweigungspunkt (84) einer dynamischen RAM-Speicherzelle (72) und das Lesen der dynamischen RAM-Zelle umfaßt.

6. Verfahren nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß der Schritt zum Anlegen eines Spannungsübergan-

ges an den zweiten Pol (20, 56, 62, 92, 110) das Steuern der Spannung an dem zweiten Pol (20, 56, 62, 92, 110) umfaßt, so daß er anfänglich auf dem ersten Spannungsniveau ist und danach auf ein anderes Niveau verändert wird.

7. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß der Schritt zum Ausbilden einer Spannung an dem gemeinsamen Verzweigungspunkt (16, 52, 58, 88, 104) das Ändern der Polarisierung von nur einem der ferroelektrischen Kondensatoren umfaßt.

8. Verfahren nach Anspruch 7, dadurch gekennzeichnet, daß der Schritt zum Ändern der Polarisierung das Steuern der Spannung an einem (18, 54, 60, 90, 108) der Pole, um konstant zu sein, umfaßt, während der Spannungsübergang an dem anderen (20, 56, 62, 92, 110) der Pole vorgesehen wird.

9. Verfahren nach Anspruch 6, dadurch gekennzeichnet, daß der Schritt zum Anlegen einer Übergangsspannung das Halten des ersten und zweiten Pols (18, 20, 54, 56, 60, 62, 90, 92, 108, 110) auf Erdniveau und anschließend das Aufbringen einer abweichenden Spannung auf den zweiten Pol (20, 56, 62, 92, 110) umfaßt, während der erste Pol (18, 54, 60, 90, 108) indes auf Erdniveau bleibt.

10. Verfahren nach Anspruch 2, dadurch gekennzeichnet, daß der Schritt zum Anlegen einer Spannung das Aufbringen einer Betriebsspannung oder einer Erdniveauspannung auf den gemeinsamen Verzweigungspunkt (16, 52, 58, 88, 104) der beiden Kondensatoren (12, 14) umfaßt, und daß der Polarisierungsschritt ferner das Steuern der Spannung an dem ersten und zweiten Pol (18, 20, 54, 56, 60, 62, 90, 92, 108, 110) der Kondensatoren (12, 14) umfaßt, so daß zwischen Erd- und Betriebsniveau gewechselt wird, während die die Daten darstellende Spannung an dem gemeinsamen Verzweigungspunkt (16, 52, 58, 88, 104) angelegt wird.

11. Verfahren nach Anspruch 10, dadurch gekennzeichnet, daß die Spannungen an die beiden Pole (18, 20, 54, 56, 60, 62, 90, 92, 108, 110), während des Polarisierungsschrittes, angelegt werden.

12. Verfahren nach einem der Ansprüche 1 oder 2, dadurch gekennzeichnet, daß der Polarisierungsschritt ferner das Speichern komplementärer Daten durch Polarisierung eines zweiten Paares in Reihe geschalteter ferroelektrischer Kondensatoren (50) umfaßt, wobei das zweite Paar Kondensatoren einen zweiten gemeinsamen Verzweigungspunkt (58) und zwei weitere Pole (60, 62) aufweist und das Polarisieren des zweiten Kondensators in entgegengesetzter Richtung als die Polarisierung des ersten Paares Kondensatoren stattfindet, und daß der Schritt zum Lesen der Daten das Erzeugen von weiteren Spannungen an dem ersten und zweiten gemeinsamen Verzweigungspunkt (52, 58) umfaßt, und daß der Erfassungsschritt das Erfassen des Unterschiedes zwischen den Spannungen an den zwei gemeinsamen Verspannungspunkten (52, 58) umfaßt.

13. Verfahren nach Anspruch 12, dadurch gekennzeichnet, daß der Polarisierungsschritt das Halten jedes Pols (54, 56, 60, 62) des ersten und zweiten Paares (48, 50) von Kondensatoren auf Erdniveau und das Ändern der Spannungen an allen Polen (54, 56, 60, 62) auf die zweite Spannung umfaßt, während komplementäre Daten darstellende Spannungen an den ersten und zweiten gemeinsamen Verzweigungspunkt (52, 58) angelegt werden.

14. Verfahren nach Anspruch 13, dadurch gekennzeichnet, daß der Erzeugungsschritt das Erden beider ersten Pole (54, 60) und das Anlegen eines Spannungsübergangs an die beiden zweiten Pole (56, 62) zusammen umfaßt.

15. Verfahren nach Anspruch 14, dadurch gekennzeichnet, daß es das Anlegen der gleichen ersten Signale an die beiden ersten Pole (54, 60) zusammen und der gleichen zweiten Signale an die beiden zweiten Pole (56, 62) enthält.

16. Verfahren nach Anspruch 12, dadurch gekennzeichnet, daß es ferner das Koppeln der beiden ersten Pole (54, 60) zusammen und das Koppeln der beiden zweiten Pole (56, 62) zusammen enthält und daß der Polarisierungsschritt das Koppeln der ersten und zweiten Pole auf Erdniveau und anschließend an eine Betriebsspannung umfaßt, und daß der Erzeugungsschritt das Koppeln der ersten Pole (54, 60) auf Erdniveau und das Anlegen eines Spannungsübergangs an die zweiten Pole (56, 62) enthält.

17. Halbleiterspeicher mit einer Speicherzelle (70, 100) und einer verbundenen Steuerschaltung (64, 94), wobei die Speicherzelle einen Kapazitätsteiler (48, 80, 106) umfaßt, der aus einem ersten und einem zweiten in Reihe geschalteten Kondensator gebildet wird, so daß ein ge-

meinsamer Verzweigungspunkt (52, 88, 104) vorgesehen ist, der mit Platten der beiden ferroelektrischen Kondensatoren gekoppelt ist, und daß ein erster (54, 90, 108) und ein zweiter (56, 92, 110) Pol vorgesehen sind, die mit den anderen beiden Platten der ferroelektrischen Kondensatoren verbunden sind, wobei der Kapazitätsteiler (48, 80, 106) einen leistungslosen Speicherzellenbereich der Speicherzelle bildet und die Steuerschaltung (64, 94) ein erstes (CLK 1, CLK 3) und ein zweites (CLK 2, CLK 4) Ausgangssignal erzeugt, die jeweils dem ersten (54, 90, 108) und dem zweiten (56, 92, 110) Pol des Kapazitätsteilers zugeführt werden, und die Anordnung derart getroffen ist, daß die Restpolarisierung des ferroelektrischen Materials in den ferroelektrischen Kondensatoren die leistungslos gespeicherten Daten darstellen, dadurch gekennzeichnet, daß die Speicherzelle ferner einen leistungsabhängigen Speicherzellenbereich (72) umfaßt, der zum Speichern von Daten auf deren inneren Verzweigungspunkt (32, 84) angeordnet ist, wobei der gemeinsame Verzweigungspunkt (52, 88, 104) des Kapazitätsteilers mit dem inneren Verzweigungspunkt (32, 84) des leistungsabhängigen Bereichs gekoppelt ist; und daß der Steuerkreis zum Erzeugen des ersten und zweiten Ausgangssignals betreibbar ist, so daß Daten in dem leistungslosen Bereich gespeichert werden durch gemeinsames Anlegen einer einem Datenzustand entsprechenden ersten Spannung an den ersten und zweiten Pol, während der gemeinsame Verzweigungspunkt (52, 88) mit dem inneren Verzweigungspunkt (32, 84) verbindbar ist, und anschließend gemeinsames Anlegen einer dem anderen Datenzustand entsprechenden zweiten Spannung an den ersten und zweiten Pol.

18. Halbleiterspeicher nach Anspruch 17, dadurch gekennzeichnet, daß der leistungsabhängige Speicherzellenbereich (72) ansprechbar mit einer Wortleitung verbunden und mit einer Bitleitung gekoppelt ist.

19. Halbleiterspeicher nach Anspruch 17, dadurch gekennzeichnet, daß der leistungsabhängige Speicherzellenbereich einen ersten (32) und einen zweiten (34) inneren Verzweigungspunkt aufweist, die mit den jeweiligen komplementären Bitleitungen gekoppelt sind und daß der leistungslose Speicherzellenbereich einen ersten (48) und einen zweiten (50) derartigen ferroelektrischen Kapazitätsteiler umfaßt, wobei die gemeinsamen Verzweigungspunkte (52, 58) des ersten und zweiten Teilers mit dem jeweiligen ersten und zweiten inneren Verzweigungspunkt gekoppelt sind und daß die Steuerschaltung (64) einen Signalgenerator umfaßt, der gekoppelt ist um ein erstes variables Signal (CLK 1) und ein zweites variables Signal (CLK 2) an ersten und zweiten Ausgängen vorzusehen, wobei das erste variable Signal und einen Pol (54) des ersten Kapazitanzteilers und einem Pol (60) des zweiten Kapazitanzteilers gekoppelt ist und das zweite variable Signal mit den anderen Polen (56, 62) des ersten und zweiten Kapazitanzteilers gekoppelt ist.

20. Halbleiterspeicher nach Anspruch 19, dadurch gekennzeichnet, daß er ferner einen ersten Koppelungstransistor (44) enthält, der einen steuerbaren Leitfähigkeitsweg aufweist, der den gemeinsamen Verzweigungspunkt (52) des ersten Kapazitanzteilers (48) mit einem (32) der inneren Verzweigungspunkte koppelt; und einen zweiten Koppelungstransistor (46) enthält, der einen steuerbaren Leitfähigkeitsweg aufweist, der den gemeinsamen Verzweigungspunkt (58) des zweiten Kapazitanzteilers (50) mit dem anderen (34) der inneren Verzweigungspunkte koppelt.

21. Halbleiterspeicher nach den Ansprüchen 19 oder 20, dadurch gekennzeichnet, daß er ferner einen ersten (35) und einen zweiten (36) Zugangstransistor und eine Wortleitung umfaßt, wobei eine der Bitleitungen mit einem ersten (32) der inneren Verzweigungspunkte durch den Source-Drain-Weg des ersten Zugangstransistors (35) gekoppelt ist und die andere der Bitleitungen mit einem zweiten (34) der inneren Verzweigungspunkte gekoppelt ist durch den Source-Drain-Weg des zweiten Zugangstransistors (36) und die Wortleitung mit den Gate-Elektroden des ersten und zweiten Zugangstransistors gekoppelt ist, wodurch die Speicherzelle ausgewählt wird, wenn die Wortleitung den ersten und zweiten Zugangstransistor einschaltet, und dadurch die Bitleitungen mit den inneren Verzweigungspunkten koppelt.

22. Halbleiterspeicher nach Anspruch 17, dadurch gekennzeichnet, daß der leistungsabhängige Speicherzellenbereich (72) mit einer Bitleitung und einer Wortleitung gekoppelt ist und einen Transistor (76) umfaßt, der mit einem Speicherkondensator (74) gekoppelt ist, wobei der innere Verzweigungspunkt (84) zwischen den Transistor (76) und den Speicherkondensator (74) geschaltet ist.

23. Halbleiterspeicher nach Anspruch 22, dadurch gekennzeichnet, daß er eine Schalteinrichtung (82) umfaßt, die einen steuerbaren Leitfähig-

keitsweg aufweist, der zwischen den gemeinsamen Verzweigungspunkt (88) und den inneren Verzweigungspunkt (84) des leistungsabhängigen Speicherzellenbereiches gekoppelt ist.

24. Halbleiterspeicher nach Anspruch 23, dadurch gekennzeichnet, daß die Schaltungseinrichtung (82) einen Feldeffekttransistor umfaßt, der eine Source, ein Drain und ein Gate umfaßt und daß der Source-Drain-Weg zwischen den gemeinsamen Verzweigungspunkt (88) und den inneren Verzweigungspunkt (84) des leistungsabhängigen Speicherzellenbereiches (72) geschaltet ist.

25. Halbleiterspeicher nach Anspruch 17, dadurch gekennzeichnet, daß der leistungsabhängige Speicherzellenbereich einen Transistor (102) umfaßt, wobei der Transistor den leistungslosen Bereich mit einer Bitleitung koppelt und der Transistor (102) ansprechbar mit einer Wortleitung gekoppelt ist.

26. Halbleiterspeicher nach Anspruch 25, dadurch gekennzeichnet, daß das ferroelektrische Material PZT umfaßt..

27. Halbleiterspeicher-Anordnung mit mehreren Speicherzellen (120, 122, 124, 126) und einer zugeordneten Steuerschaltung, wobei jede Speicherzelle einen leistungslosen Speicherzellenbereich umfaßt, der einen Kapazitätsteiler (48, 80, 106) enthält, welcher durch einen ersten und einen zweiten in Reihe geschalteten ferroelektrischen Kondensator gebildet wird, so daß ein gemeinsamer Verzweigungspunkt (53, 88, 104) vorgesehen wird, der mit Platten von beiden ferroelektrischen Kondensatoren gekoppelt ist, und daß ein erster (54, 90, 108) und ein zweiter (56, 92, 110) Pol vorgesehen sind, die mit den anderen beiden Platten der ferroelektrischen Kondensatoren verbunden sind, wobei die Speicheranordnung umfaßt:
mehrere Bitleitungen (134,136), die Spalten festlegen; mehrere Wortleitungen (130, 132), die Reihen orthogonal zu den Bitleitungen festlegen;
wobei die Speicherzellen (120, 122, 124, 126) an Kreuzungen der Wortleitungen, der Bitleitungen und jeder Zelle angeordnet sind, gekennzeichnet durch einen leistungsabhängigen Speicherzellenbereich, der mit dem gemeinsamen Verzweigungspunkt des leistungslosen Speicherzellenbereichs gekoppelt ist, und dadurch, daß dies Speicheranordnung ferner mehrere Paare an leitfähigen, gemeinsamen Leitungen (138, 140, 142, 144) umfaßt, und ein Paar (138, 140) mit einer der Wortleitungen (130) korrespondiert, wobei eine der gemeinsamen Leitungen (138) des Paares mit den ersten Polen (54, 90, 108) in den Speicherzellen entlang der Reihe gekoppelt ist und die andere (140) der gemeinsamen Leitungen des Paares mit den zweiten Polen (56, 92, 110) in den Speicherzellen entlang der Reihe gekoppelt ist, unterschiedliche Spannungen getrennt entlang einer ausgewählten Reihe an die ersten und zweiten Pole anlegbar sind, und die verbundene Steuerschaltung derart betrieben werden kann, daß sie unterschiedliche Spannungen erzeugt, um Daten im leistungslosen Bereich zu speichern durch gemeinsames Anlegen einer ersten einem Datenzustand entsprechenden Spannung an den ersten und zweiten Pol, während der gemeinsame Verzweigungspunkt (52, 88, 104) mit dem inneren Verzweigungspunkt (32, 34) verbindbar ist, und anschließend gemeinsames Anlegen einer zweiten, dem anderen Datenzustand entsprechenden Spannung an beiden, dem ersten und zweiten Pol.

28. Anordnung eines Halbleiterspeichers nach Anspruch 27, dadurch gekennzeichnet, daß jeder der leistungsabhängigen Speicherzellenbereiche einen Feldeffekttransistor umfaßt, der eine Gate-Elektrode aufweist, die mit entsprechenden Wortleitungen (130, 132) gekoppelt ist und der Source-Drain-Weg des Transistors die entsprechende Bitleitung (134, 136) mit dem entsprechenden gemeinsamen Verzweigungspunkt koppelt.

29. Anordnung eines Halbleiterspeichers nach Anspruch 27 oder 28, dadurch gekennzeichnet, daß die verbundene Steuerschaltung (64, 94) einen Signalgenerator umfaßt, der mindestens ein auswählbar variables Signal (CLK 1) vorsieht, das durch eine (138) des Paares leitfähiger gemeinsamer Leitungen mit einem Pol des Kapazitätsteilers gekoppelt ist.

Revendications

1. Procédé pour lire et inscrire des données numériques dans une mémoire rémanente comprenant les étapes suivantes:

inscription des données numériques en polarisant une première paire de condensateurs ferroélectriques (12, 14) couplés en série, ladite première paire de condensateurs ayant un noeud commun (16, 52, 58, 88, 104) et des premiers et seconds pôles (18, 20, 54, 56, 60, 62, 90, 92, 108, 110), pour polariser le matériau ferroélectrique dans les condensateurs en correspondance avec les données; et

lecture des données en développant une tension audit noeud commun (16, 52, 58, 88, 104) en appliquant une transition de tension uniquement à l'un (20, 56, 62, 92, 110) desdits pôles; caractérisé par l'étape de détection de ladite tension audit noeud commun (16, 52, 58, 88, 104), et en ce que ladite étape de polarisation consiste à appliquer une tension représentant les données audit noeud commun (16, 52, 58, 88, 104) tout en appliquant une première tension correspondant à un état de données auxdits deux pôles (18, 20, 54, 56, 60, 62, 90, 92, 108, 110) ensemble, puis à appliquer une seconde tension correspondant à l'autre état de données auxdits deux pôles (18, 20, 54, 56, 60, 62, 90, 92, 108, 110) ensemble.

2. Procédé selon la revendication 1, dans lequel ladite étape de lecture de données consiste à maintenir ledit premier pôle (18, 54, 60, 90, 108) à ladite première tension tout en appliquant une transition de tension audit second pôle (20, 56, 62, 92, 110), ladite tension développée étant indicatrice desdites données numériques.

3. Procédé selon la revendication 1 ou 2, dans lequel ladite tension appliquée audit noeud commun (16, 52, 58, 88, 104) au cours de ladite étape de polarisation est soit à la masse, soit à un niveau de fonctionnement, et dans lequel lesdites première et seconde tensions comportent la masse et une tension de fonctionnement.

4. Procédé selon l'une quelconque des revendications précédentes, dans lequel ladite étape d'application comporte le couplage d'un noeud interne (32, 84) d'une cellule (72) de mémoire non rémanente audit noeud commun (52, 88).

5. Procédé selon l'une quelconque des revendications 1 à 3, dans lequel ladite étape de détection comporte le couplage dudit noeud commun (88) à un noeud interne (84) d'une cellule (72) de mémoire RAM dynamique et la lecture de ladite cellule de mémoire RAM dynamique.

6. Procédé selon l'une quelconque des revendications précédentes, dans lequel l'étape d'application d'une transition de tension audit second pôle (20, 56, 62, 92, 110) consiste à commander la tension sur ledit second pôle (20, 56, 62, 92, 110) de telle sorte qu'il soit initialement à ladite première tension puis qu'il passe à un autre niveau.

7. Procédé selon la revendication 1, dans lequel ladite étape de développement d'une tension audit noeud commun (16, 52, 58, 88, 104) consiste à modifier la polarisation de seulement l'un desdits condensateurs ferroélectriques.

8. Procédé selon la revendication 7, dans lequel ladite étape de modification de la polarisation consiste à commander la tension sur l'un (18, 54, 60, 90, 108) desdits pôles pour être constante tout en établissant ladite transition de tension sur l'autre (20, 56, 62, 92, 110) desdits pôles.

9. Procédé selon la revendication 6, dans lequel ladite étape d'application d'une transition de tension consiste à maintenir lesdits premiers et seconds pôles (18, 20, 54, 56, 60, 62, 90, 92, 108, 110) à la masse, puis à imprimer une tension différente sur ledit second pôle (20, 56, 62, 92, 110) tandis que ledit premier pôle (18, 54, 60, 90, 108) est encore à la masse.

10. Procédé selon la revendication 2, dans lequel ladite étape d'application d'une tension consiste à appliquer une tension de fonctionnement ou une tension au niveau de la masse audit noeud commun (16, 52, 58, 88, 104) desdits deux condensateurs (12, 14) et ladite étape de polarisation consiste en outre à commander la tension auxdits premiers et seconds pôles (18, 20, 54, 56, 60, 62, 90, 92, 108, 110) desdits condensateurs (12, 14) pour passer de la masse au niveau de fonctionnement tandis que ladite tension représentant les données est appliquée audit noeud commun (16, 52, 58, 88, 104).

11. Procédé selon la revendication 10, dans lequel les tensions sont appliquées auxdits pôles (18, 20, 54, 56, 60, 62, 90, 92, 108, 110) ensemble au cours de ladite étape de polarisation.

12. Procédé selon la revendication 1 ou 2, dans lequel l'étape de polarisation consiste en outre à stocker des données complémentaires en polarisant une seconde paire de condensateurs ferroélectriques (50) couplés en série, ladite seconde paire de condensateurs ayant un second noeud commun (58) et deux autres pôles (60, 62), ladite polarisation de ladite seconde paire de condensateurs se faisant dans le sens opposé à la polarisation de ladite première paire de condensateurs, et dans lequel ladite étape de lecture des données consiste à générer d'autres tensions auxdits premier et second noeuds communs (52, 58), et dans lequel ladi-

te étape de détection consiste à détecter la différence entre les tensions auxdits deux noeuds communs.

13. Procédé selon la revendication 12, dans lequel ladite étape de polarisation consiste à maintenir chaque pôle (54, 56, 60, 62) desdites première et seconde paires (48, 50) de condensateurs à la masse et à faire passer la tension sur tous lesdits pôles (54, 56, 60, 62) à ladite seconde tension tout en appliquant des tensions représentant des données complémentaires auxdits premier et second noeuds communs (52, 58).

14. Procédé selon la revendication 13, dans lequel ladite étape de génération consiste à relier à la masse lesdits deux premiers pôles (54, 60) et à appliquer une transition de tension auxdits seconds pôles (56, 62) ensemble.

15. Procédé selon la revendication 14, consistant à appliquer les mêmes premiers signaux auxdits premiers pôles (54, 60) ensemble et les mêmes seconds signaux auxdits seconds pôles (56, 62) ensemble.

16. Procédé selon la revendication 12, consistant en outre à coupler lesdits premiers pôles (54, 60) ensemble et à coupler lesdits seconds pôles (56, 62) ensemble, et dans lequel ladite étape de polarisation consiste à coupler lesdits premiers et seconds pôles à la masse puis à une tension de fonctionnement, et dans lequel ladite étape de génération consiste à coupler lesdits premiers pôles (54, 60) à la masse et à appliquer une transition de tension auxdits seconds pôles (56, 62).

17. Mémoire semiconductrice comprenant une cellule de mémoire (70, 100) et un circuit de commande associé (64, 94), la cellule de mémoire comprenant un diviseur de tension capacitif (48, 80, 106) formé par des premier et second condensateurs ferroélectriques en série pour obtenir un noeud commun (52, 88, 104) couplé aux plaques des deux condensateurs ferroélectriques et pour obtenir des premiers (54, 90, 108) et seconds (56, 92, 110) pôles couplés aux deux autres plaques desdits condensateurs ferroélectriques, dans laquelle le diviseur de tension capacitif (48, 80, 106) forme une partie de cellule de mémoire rémanente de la cellule de mémoire, et dans laquelle ledit circuit de commande (64, 94) délivre des premiers (CLK1, CLK3) et des seconds (CLK2, CLK4) signaux de sortie appliqués respectivement aux premiers (54, 90, 108) et aux seconds (56, 92, 110) pôles dudit diviseur de tension capacitif, l'agencement étant tel que la polarisation rémanente du matériau ferroélectrique dans lesdits condensateurs ferroélectriques représente les données stockées rémanentes, caractérisée en ce que la cellule de mémoire comporte en outre une partie (72) de cellule de mémoire volatile agencée pour stocker des données sur un de ses noeuds internes (32, 84), ledit noeud commun (52, 88, 104) dudit diviseur de tension capacitif étant couplé audit noeud interne (32, 84) de ladite partie volatile; et en ce que ledit circuit de commande peut fonctionner pour produire lesdits premiers et seconds signaux de sortie pour conduire les données à être stockées dans ladite partie rémanente en appliquant une première tension correspondant à un état de données auxdits premiers et seconds pôles ensemble tout en permettant au noeud commun (52, 88, 104) d'être connecté audit noeud interne (32, 84), puis en appliquant une seconde tension correspondant à l'autre état de données auxdits premiers et seconds pôles ensemble.

18. Mémoire semiconductrice selon la revendication 17, dans laquelle ladite partie (72) de cellule de mémoire volatile est couplée de manière sensible à une ligne de mots et est couplée à une ligne de bits.

19. Mémoire semiconductrice selon la revendication 17, dans laquelle la partie de cellule de mémoire volatile comporte des premier (32) et second (34) noeuds internes, couplés à des lignes de bits complémentaires respectives et dans laquelle la partie de cellule de mémoire rémanente comporte des premier (48) et second (50) diviseurs de tension à condensateur ferroélectrique, lesdits noeuds communs (52, 58) desdits premier et second diviseurs étant couplés auxdits premiers et seconds noeuds internes respectivement, ledit circuit de commande (64) comprenant un générateur de signaux couplé pour délivrer un premier signal variable (CLK1) et un second signal variable (CLK2) sur des première et seconde sorties, ledit premier signal variable étant couplé à un pôle (54) dudit premier diviseur de tension capacitif et à un pôle (60) dudit second diviseur de tension capacitif et le second signal variable étant couplé aux autres pôles (56, 62) desdits premier et second diviseurs de tension capacitifs.

20. Mémoire semiconductrice selon la revendication 19, comprenant en outre un premier tran-

sistor de couplage (44) ayant un trajet de conductivité commandable couplant ledit noeud commun (52) dudit premier diviseur de tension capacitif (48) à l'un (32) desdits noeuds internes; et

un second transistor de couplage (46) ayant un trajet de conductivité commandable, couplant ledit noeud commun (58) dudit second diviseur de tension capacitif (50) à l'autre (34) desdits noeuds internes.

21. Mémoire semiconductrice selon la revendication 19 ou 20, comprenant en outre un premier (35) et un second (36) transistors d'accès, et une ligne de mots, l'une desdites lignes de bits étant couplée à un premier (32) desdits noeuds internes par l'intermédiaire du trajet source-drain dudit premier transistor d'accès (35), l'autre desdites lignes de bits étant couplée à un second (34) desdits noeuds internes par le trajet source-drain dudit second transistor d'accès (36), ladite ligne de mots étant couplée aux électrodes de grille desdits premier et second transistors d'accès, de telle sorte que ladite cellule de mémoire soit sélectionnée lorsque ladite ligne de mots met en circuit lesdits premier et second transistors d'accès afin de coupler les lignes de bits auxdits noeuds internes.

22. Mémoire semiconductrice selon la revendication 17, dans laquelle ladite partie (72) de cellule de mémoire volatile est couplée à une ligne de bits et à une ligne de mots et comporte un transistor (76) couplé à un condensateur de mémorisation (74), ledit noeud interne (84) étant connecté entre ledit transistor (76) et ledit condensateur de mémorisation (74).

23. Mémoire semiconductrice selon la revendication 22, comportant un dispositif de commutation (82) ayant un trajet de conductivité commandable couplé entre ledit noeud commun (88) et ledit noeud interne (84) de la partie de cellule de mémoire volatile.

24. Mémoire semiconductrice selon la revendication 23, dans laquelle ledit dispositif de commutation (82) comporte un transistor à effet de champ ayant une source, un drain et une grille, et dans laquelle ledit trajet source-drain est couplé entre ledit noeud commun (88) et ledit noeud interne (84) de la partie (72) de cellule de mémoire volatile.

25. Mémoire semiconductrice selon la revendication 17, dans laquelle ladite partie de cellule de mémoire volatile comporte un transistor (102), ledit transistor couplant ladite partie rémanente à une ligne de bits, et ledit transistor (102) étant couplé de manière sensible à une ligne de mots.

26. Mémoire semiconductrice selon la revendication 25, dans laquelle ledit matériau ferroélectrique comporte du PZT.

27. Réseau de mémoire semiconductrice comprenant une pluralité de cellules de mémoire (120, 122, 124, 126) et un circuit de commande associé les cellules de mémoire comprenant chacune une partie de cellule de mémoire rémanente comportant un diviseur de tension capacitif (48, 80, 106) formé par des premier et second condensateurs ferroélectriques en série pour fournir un noeud commun (52, 88, 104) couplé à des plaques des deux condensateurs ferroélectriques et pour fournir des premiers (54, 90, 108) et des seconds (56, 92, 110) pôles couplés aux deux autres plaques desdits condensateurs ferroélectriques, le réseau de mémoire comportant:

une pluralité de lignes de bits (134, 136) définissant des colonnes;

une pluralité de lignes de mots (130, 132) définissant des rangées orthogonales auxdites lignes de bits;

ladite pluralité de cellules de mémoire (120, 122, 124, 126) étant située aux croisements desdites lignes de mots et desdites lignes de bits et chaque cellule étant caractérisée en ce qu'elle comporte une partie de cellule de mémoire volatile couplée au noeud commun de la partie de cellule de mémoire rémanente; et

ledit réseau de mémoire comportant en outre une pluralité de paires de lignes communes conductrices (138, 140, 142, 144), une paire (138, 140) correspondant à l'une desdites lignes de mots (130), dans laquelle l'une desdites lignes communes (138) de la paire est couplée auxdits premiers pôles (54, 90, 108) dans lesdites cellules de mémoire le long de la rangée, et l'autre (140) desdites lignes communes de la paire étant couplée auxdits seconds pôles (56, 92, 110) dans les cellules de mémoire le long de la rangée, afin que des tensions distinctes puissent être appliquées auxdits premiers et seconds pôles séparément le long d'une rangée sélectionnée; de manière que ledit circuit de commande associé puisse fonctionner pour produire lesdites tensions distinctes pour conduire les données à être stockées dans ladite partie rémanente en appliquant une première tension correspondant à un état de données auxdits premiers et se-

conds pôles ensemble tout en permettant au noeud commun (52, 88, 104) d'être connecté audit noeud interne (32, 84), puis en appliquant une seconde tension correspondant à l'autre état de données auxdits premiers et seconds pôles ensemble.

28. Réseau de mémoire semiconductrice selon la revendication 27, dans lequel lesdites parties de cellule de mémoire volatile comprennent chacune un transistor à effet de champ ayant une électrode de grille couplée aux lignes de mots correspondantes (130, 132), le trajet source-drain dudit transistor couplant ladite ligne de bits correspondante (134, 136) au noeud commun correspondant.

29. Mémoire semiconductrice selon la revendication 27 ou la revendication 28, dans laquelle ledit circuit de commande associé (64, 94) comporte un générateur de signaux délivrant au moins un signal sélectivement variable (CLK1) couplé par l'une (138) de ladite paire de lignes communes conductrices à un pôle dudit diviseur de tension capacitif.

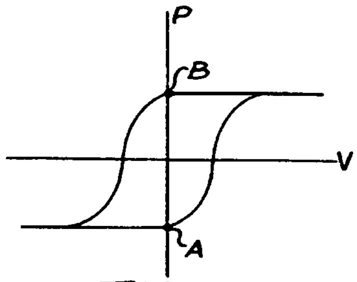


FIG. 1

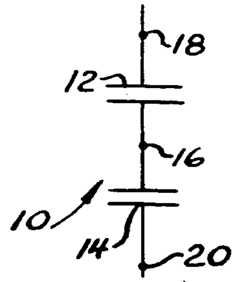


FIG. 2A

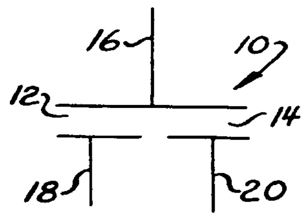


FIG. 2B

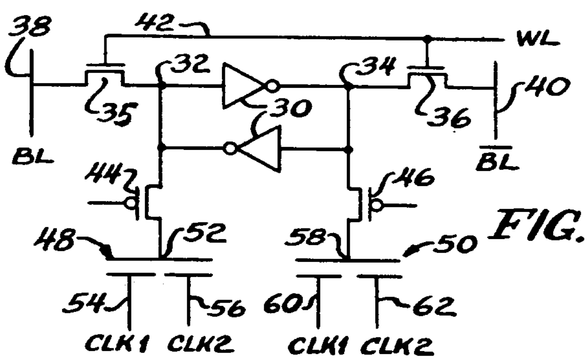


FIG. 3A

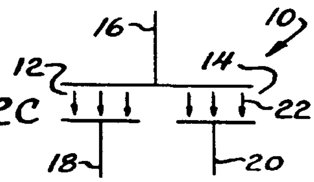


FIG 2C

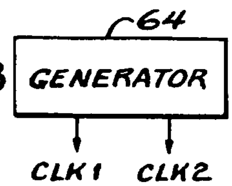


FIG. 3B

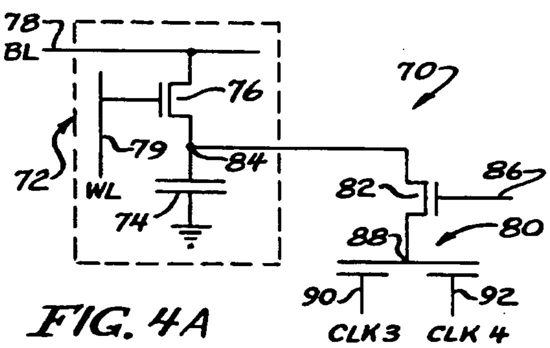
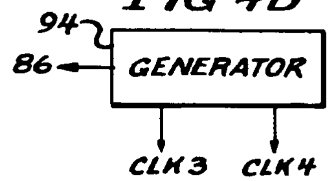


FIG. 4A

FIG 4B


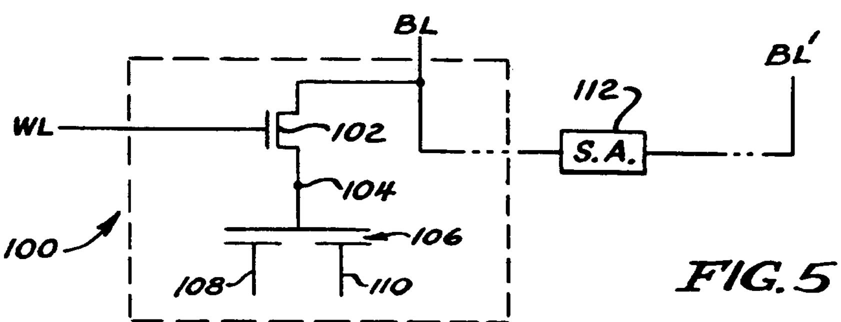


FIG. 5

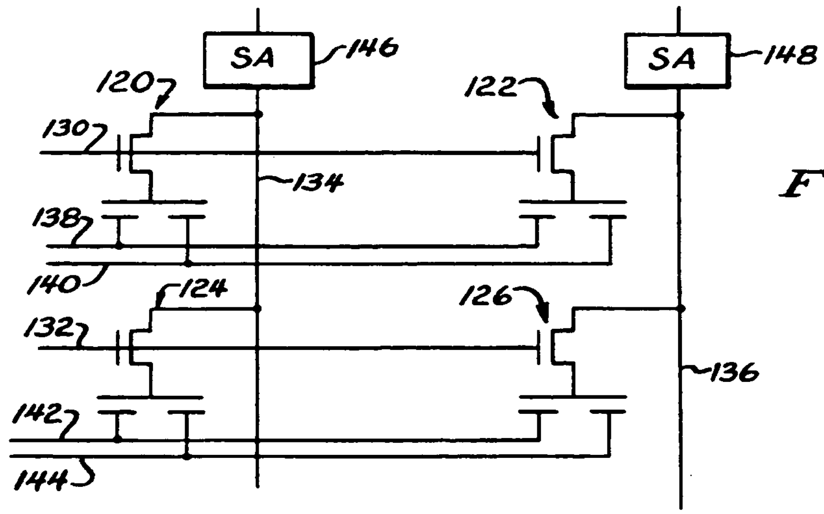


FIG. 6

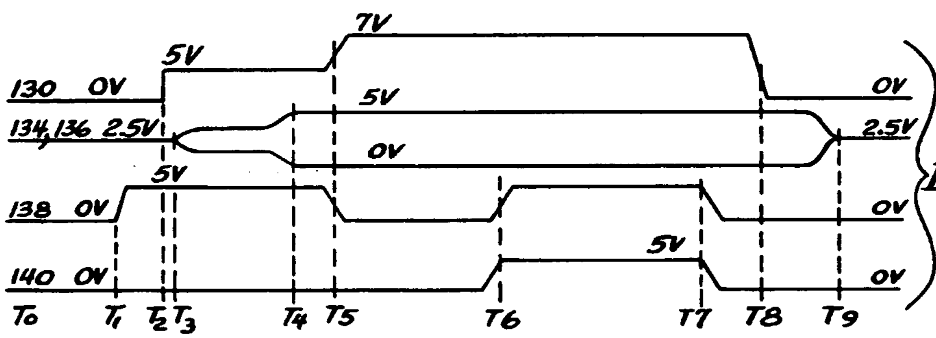


FIG. 7

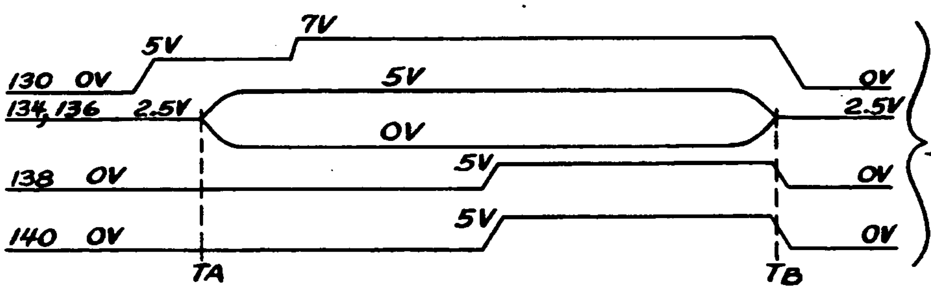


FIG. 8

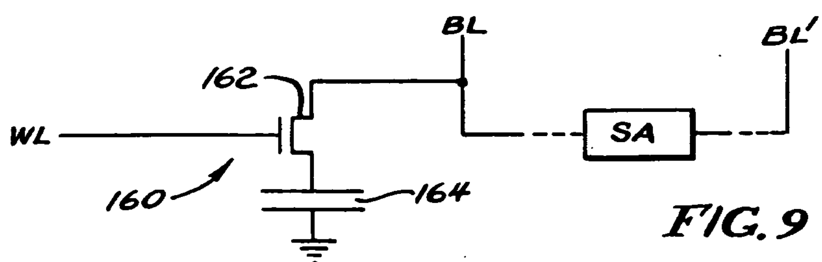


FIG. 9